EXHIBIT K

HIGH-VOLTAGE DMOS AND PMOS IN ANALOG IC'S

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ABSTRACT

A lateral 300V DMOS device is described which can be integrated in a standard bipolar IC process. The device, applicable as a high voltage source follower for analog circuits, is based upon the "double-acting resurf" principle; a modification with an interrupted p- top layer or with a stepped field plate is used. The p- layer improves the interconnection-induced breakdown and can be used in the extended drain of a 280 V PMOST.

INTRODUCTION

For functions like driving transducers or CRT's and for analog switches, high voltage analog stages of over 250 V may be needed on the chip. Vertical bipolars are less suitable because of the required thick epi-layers and even integration of vertical DMOS devices in a standard IC process is rather difficult. High voltage lateral MOS devices of over 500 V, using thin layer extended drain or "resurf" techniques (1-3), can easily be incorporated, but a high voltage source follower is impossible. Source followers using lateral DMOS devices and 25-30 μm epi have been reported (4); here 200 V is considered the limit for junction isolated devices because of deep isolation diffusions and parasitic bulk and surface effects (5). Recently a "double-acting resurf" technique has been reported (6); compared to "resurf" as mentioned above, it not only offers better lateral conduction but also prevention of substrate punch-through in follower applications. Owing to a higher doping content of the n layer (about 2.10^{12} cm^{-2}), the depletion layer at source (back gate)-to-substrate breakdown does not extend to the surface diffusion (as shown by the left-hand shaded area in fig. 1) and no punch-through occurs. At high voltage on the n^+ drain with the other terminals grounded, a high field would occur at the source edge. By using a p-top layer, depletion of the n layer is obtained from the top and the bottom (right-hand shaded areas in fig. 1) causing a smooth voltage decrease over the lateral distance between source and drain; at high drain voltage this p- top layer has to be depleted too. The effect was demonstrated on JFET and lateral bipolar devices (6); the p_2 and n layers were optimized at 0.5 10^{12} cm^{-2} and 1.8 10^{12} cm^{-2} respectively.

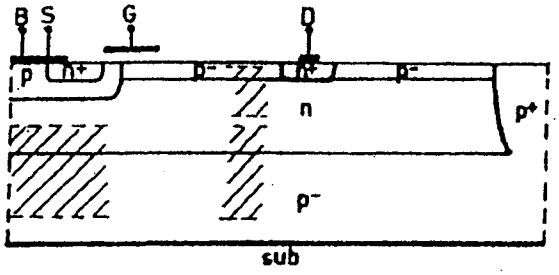

Fig.1. A double-acting resurf structure.

LATERAL DMOST

For proper functioning of a lateral DMOST (LDMOST), the design of fig. 1 has to be adapted. In fig. 2 a window is shown, made locally in the p-layer at the source side; electrons from the gate-controlled surface channel now pass through a vertical JFET which limits the current capability and increases the on-resistance. The window dimensions are therefore a compromise between on-resistance and breakdown.

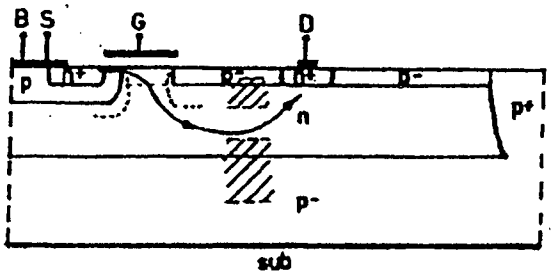

Fig.2. LDMOST with interrupted p-layer.

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Instead of a p-top layer also a stepped field plate, connected to gate or source, can be applied in order to obtain depletion from the surface, as shown in fig. 3.

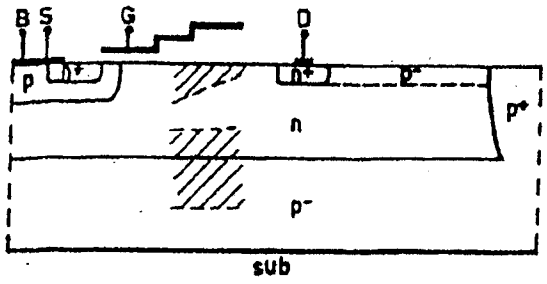


Fig.3. LDMOST with stepped field plate.

The pinching effect on the n layer is much less, lowering the breakdown voltage, but now the entire epi-layer with local accumulation contributes to a low on-resistance.

Computer calculations using our 2D Poisson-program "Semmy" were performed on the structure depicted in fig. 4 for several combinations of p-layer and field plates, cf. table 1. A 19 µm 5Ωcm n-type epi-layer as used in a 50-60 V standard bipolar process is applied on a 30Ωcm p-substrate. The 3 µm p-layer, assumed without a window here, has a net dose of $6\ 10^{12}$ cm^{-2}; this high value improves the current capability of an extended drain PMOST as will be discussed later on,

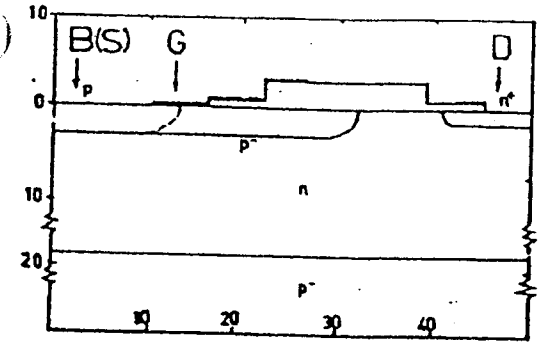


Fig.4. LDMOST structure; dimensions in µm.

but delays pinch off and requires the p-layer to be withdrawn from the n^+ drain in order to prevent low breakdown values. The gate-oxide is 0.1 µm; the field plates (dashed) step on 0.8 and 3.0 µm oxide. The punch-through voltage to the substrate is calculated to be 600V; spreading of epi dope and thickness may decrease this value to 300 V.

In figs. 5 and 6 equipotential and equifield lines at 300 V drain voltage are shown for a device with a p-layer; the co-operation of top and bottom depletion is visible on the left in fig. 5. The highest field of 23.2 V/µm, obtained at the p-diffusion curvature, does not cause breakdown (avalanche integral <1).

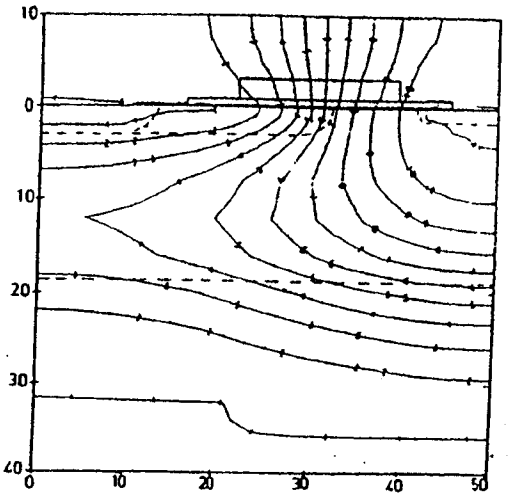


Fig.5. LDMOST equipotential lines at V d-s = 300V; per step 30V, step 1=0V.

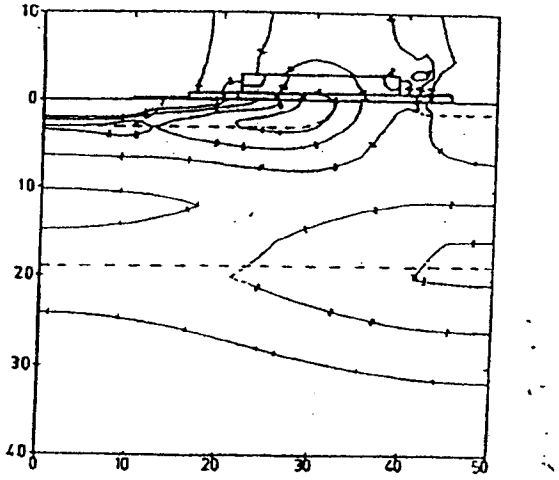


Fig.6. LDMOST equifield lines at V d-s = 300V; per step 5V/µm, step 1=5V/µm.

Table 1 E max (in V/µm) at V d-s=300V; epi, p-layer and field plates (F.P.) as in fig. 4.

substr.	p-	F.P.	E_{maxSi}	B.V.	E_{maxox}
n	yes	yes	32.0	<300	56
p-	no	no	63.5	<<300	177
p-	yes	no	23.2	>300	22.7
p-	no	yes	28.7	>300	95
p-	yes	yes	24.5	>300	35

Fig.7 shows an actual device with a stepped field plate connected to the source; the layout corners are bevelled. At the connection of the polysilicon gate th e field plate had to be interrupted as single-layer metallization is used and a local p-layer is applied. The active gate width is 500 µm, the channel length is approx. 2.0 µm. The drain surrounds the back gate and prevents parasitic PMOS action from back gate to isolation when the source is at high voltage. As crossing interconnection over shallow n^+ shows only 200V breakdown on 3.0 µm oxide, the shallow n^+ drain has been locally omitted underneath this metallization. A collector wall diffusion

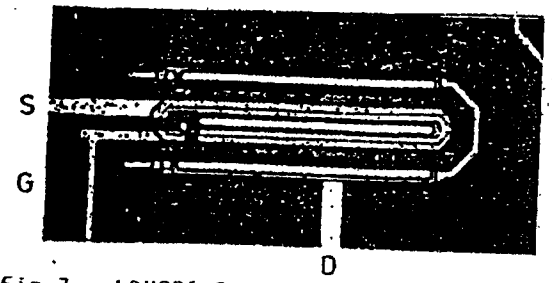


Fig.7. LDMOST for 300V; gate and source with field plate in the centre, n^+ drain 3/4 around as a stopper; drain pitch 90 µm.

or a buried polysilicon field shield can be used here; this way a breakdown >300 V is obtained. At the isolation diffusion edge a p-layer is applied (withdrawn from the n^+ drain), which improves breakdown noticeably in the case of crossing (drain) interconnection and avoids walk-out phenomena below 300V.

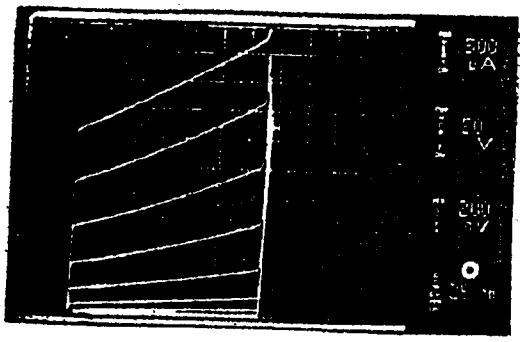


Fig.8. LDMOST BV drain-to-source; the substrate is connected to the source.

A source-to-substrate breakdown of over 300V was obtained limited by the drain-to-isolation distance. Drain-to-source breakdown (substrate is at source potential) is shown in fig. 8 to be over 300V; breakdown generally occurs at the bevelled back gate corners.

Fig. 9 shows the low-voltage on-characteristics. V_T is about 2.4V and β_o=16 µA/V^2. R_{on} is 300 Ω corresponding with 6.7 Ω-mm^2 for the active area. Owing to partial depletion of the epi-layer, R_{on} increases at 300 V s-sub to 450 Ω and I_{max} (10V d-s) becomes 18mA. For a variant according to fig. 2 with a p-ring and 10 µm local windows R_{on} was found to be 450-600 Ω.

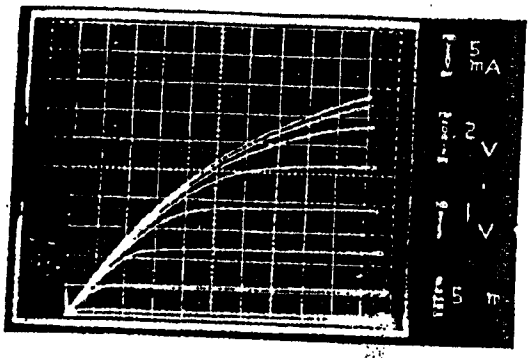


Fig.9. LDMOS on-characteristics.

Experiments in plastic encapsulation showed good stability in dry ambient at 150°C. In wet ambient instabilities are sometimes observed at the drain. Simulation with a field plate at V_{surf} on 1 µm nitride on top of the structure indicated the drain configuration of fig. 4 to be poor; a field plate overlapping the n^+ drain edge is sufficient.

EXTENDED DRAIN PMOST

In the same process a complementary high-voltage extended drain PMOST (EPMOST) has been made; the extension is pinched between the epi-layer and a stepped field plate connected to source or gate (cf. ref.7). For better gradual pinching and less Early effect in the PMOS channel, a buried n^+ layer is applied locally as shown in fig. 10. Source and back gate are

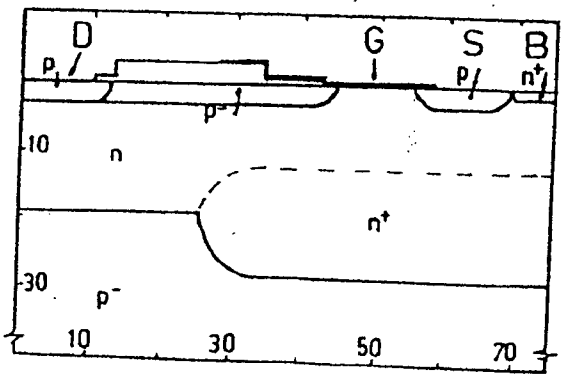


Fig.10. Extended drain PMOST structure.

situated on the right, drain and p- extension on the left. The effective channel length is about 11 μm, but lower values with more Early-effect are possible. A computer calculation with 300V on source and gate shows equipotential and equifield lines (figs. 11 and 12); the maximum field of 23V/μm does not cause breakdown. An actual EPMOST is shown in fig. 13; the p drain is in the centre and the n^+ backgate contact on the outside of the device acts as a stopper for parasitic PMOS action.

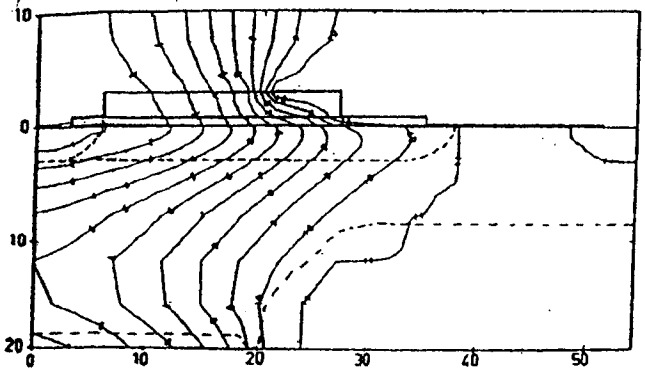


Fig. 11. EPMOST equipotential lines at V s, g-d, sub=300V; per step 30V, step 1=0V.

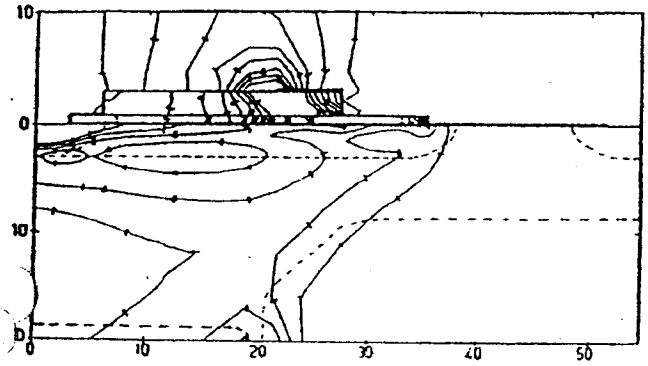
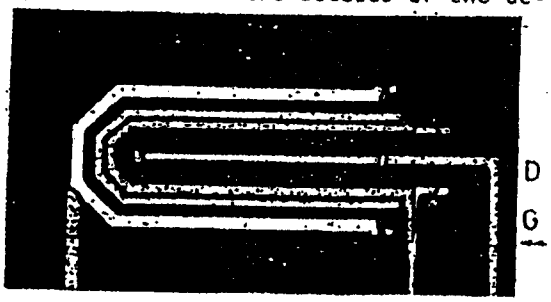


Fig. 12. EPMOST equifield lines at V s, g-d, sub=300V; per step 5V/μm, step 1=5V/μm.



ig. 13. EPMOST with central drain and gate, source and back gate 3/4 around; the n^+ back gate acts as a stopper; scale as fig. 7.

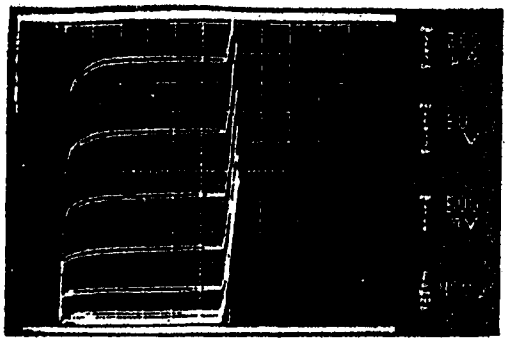


Fig. 14. EPMOST 8V drain-to-source; the substrate is connected to the drain.

The measured drain-to-source breakdown is shown in fig. 14 to be 280V; this breakdown occurs at the small-radius end of the drain. The active gate width is about 550 μm; V_T=1.5V, g_m max ($10V_{d-s}$)=1.4mA/V and β_o=7μA/V^2.R_{oo} is 900 Ω, corresponding with 30Ωmm for the active area.

CONCLUSION

By using a modification of the "double-acting resurf" principle, a lateral DMOST for 300V analog applications can be integrated with standard bipolar components. The use of a p- implanted layer allows interconnections to over 300V on 3 μm oxide. The same p-layer has been used in an extended drain PMOST of 280V.

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